Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A register controlled delayed lock loop for use in a semiconductor memory device, comprising:

a delay line having a plurality of delay cell [[unit]] units for delaying [[an]] a non-delayed input clock signal;

a delay model, which receives the signal outputted from the delay line, for reflecting a delay condition for an actual clock signal path of the non-delayed input clock signal passing through the delay line;

a delay means for delaying an output signal of the delay model for a predetermined time;

an acceleration mode delay controller for controlling the delay value in an acceleration mode according to operation frequency information;

a first phase comparator for comparing a phase of the output signal provided from the delay model with that of the non-delayed input clock signal;

a second phase comparator for comparing a phase of the output signal of the delay means with that of the non-delayed input clock signal;

a mode decision means for determining a continuous execution or termination of[[:]] [[an]] the acceleration mode in response to output signals of the first and second phase comparators;

a shift register control means for outputting a left shift signal, a right shift signal and an acceleration shift signal in response to output signals of the first phase comparator and the mode decision means; and

a shift register for controlling a delay value of the delay line in response to an output signal of the shift register control means.

Claim 2 (currently amended). The register controlled delayed lock loop as recited in claim 1 wherein a delay value of the delay means is the same [[to]] as that of the delay line increased in response to the acceleration shift signal.

Claim 3 (currently amended). The register controlled delayed lock loop as recited in claim 2, wherein the shift register includes:

a plurality of latches, each having a reset terminal, an output terminal and a sub-output terminal;

a plurality of first switches for supplying a value of the latch to a neighboring latch on the left in response to the left shift signal;

a plurality of second switches for supplying a value of the latch to a neighboring latch on the right in response to the right shift signal; and

a plurality of third switches for supplying a value of the latch to another latch separated with a predetermined distance in response to the [[left]] acceleration shift signal.

Claim 4 (cancelled).

Claim 5 (cancelled).

Claim 6 (original). The register controlled delayed lock loop as recited in claim 2, wherein the delay value of the delay means is a multiplication of the delay value of the delay cell unit by a predetermined times.

Claim 7 (currently amended). The register controlled delayed lock loop as recited in claim 6, wherein the delay value of the delay means is smaller than a ~~value dividing a frequency~~ half period of the non-delayed input clock signal.

Claim 8 (currently amended). A semiconductor memory device including a delay locked loop, comprising:

a delay line having a plurality of delay cell [[unit]] units for delaying [[an]] a non-delayed input clock signal;

a delay model, which receives the signal outputted from the delay line, for reflecting a delay condition for an actual clock signal path of the non-delayed input clock signal passing through the delay line;

a delay means for delaying an output signal of the delay model for a predetermined time;

an acceleration mode delay controller for controlling the delay value in an acceleration mode according to operation frequency information;

a first phase comparator for comparing a phase of the output signal provided from the delay model with that of the non-delayed input clock signal;

a second phase comparator for comparing a phase of the output signal of the delay means with that of the non-delayed input clock signal;

a mode decision means for determining a continuous execution or termination of [[an]] the acceleration mode in response to output signals of the first and second phase comparators;

a shift register control means for outputting a left shift signal, a right shift signal and an acceleration shift signal in response to output signals of the first phase comparator and the mode decision means; and

a shift register for controlling a delay value of the delay line in response to an output signal of the shift register control means.

Claim 9 (currently amended). The semiconductor memory device of claim 8, wherein a delay value of the delay means is the same [[to]] as that of the delay line increased in response to the acceleration shift signal.

Claim 10 (currently amended). The semiconductor memory device of claim 8, wherein the shift register includes:

a plurality of latches, each having a reset terminal, an output terminal and a sub-output terminal;

a plurality of first switches for supplying a value of the latch to a neighboring latch on the left in response to the left shift signal;

a plurality of second switches for supplying a value of the latch to a neighboring latch on the right in response to the right shift signal; and

a plurality of third switches for supplying a value of the latch to another latch separated with a predetermined distance in response to the [[left]] acceleration shift signal.

Claim 11 (cancelled).

Claim 12 (cancelled).

Claim 13 (original). The semiconductor memory device of claim. 9, wherein the delay value of the delay: means is a multiplication of the delay value of the delay cell unit by a predetermined times.

Claim 14 (currently amended). The semiconductor memory device of claim 13, wherein the delay value of the delay means is smaller than a ~~value dividing a frequency~~ half period of the non-delayed input clock signal.

Claim 15 (cancelled).

Claim 16 (currently amended). The register controlled delayed lock loop as recited in claim [[15]]1, the operation frequency information is generated by using a column address strobe latency (CAS latency).

Claim 17 (original). The register controlled delayed lock loop as recited in claim 16, the operation frequency information is generated by using a mode register setting value in case of synchronous semi-conductor memory device.